Appl. No. 10/606,702
Examiner: Wojciechowicz, Edward J., Art Unit 2815
In response to the Office Action dated August 10, 2004

Date: November 3, 2004
Attorney Docket No. 10112301

REMARKS

Responsive to the Office Action mailed on August 10, 2004 in the above-referenced application, Applicant respectfully requests amendment of the above-identified application in the manner identified above and that the patent be granted in view of the arguments presented. No new matter has been added by this amendment.

Present Status of Application

Claims 1-25 are pending. Claims 14-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (US 5,828,602). Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Lin et al (US 2004/0057328).

In this paper, claims 1 and 14 are amended to recite that the conducting spacer is tapered to a point at the gate dielectric layer. Support for these amendments can be found on page 7, line 28 to page 8, lines 3 and Figs. 2i and 2j of the application. Claim 14 is further amended to delete the limitation "wherein the conducting spacer electrically connected to the source conducting layer and the conducting spacer". Claims 7, 19 and 26-33 are canceled.

Reconsideration of this application is respectfully requested in light of the amendments and the remarks contained below.

Foreign Priority Claim

Acknowledgment of Applicant's claim to foreign priority under 35 USC 119(a)-(d) or (f) and receipt of the certified copy of the priority document is respectfully requested. Applicant notes that the priority document was received by the Office on June 26, 2003.

Rejections under 35 U.S.C. 112

Claims 14-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Applicant has deleted the limitation identified by the office action as indefinite.

Applicant submits that the rejections of claims 14-25 under 35 U.S.C. 112 are thereby overcome.

Rejections under 35 U.S.C. 102(b)

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong. To the extent that they are applicable to the claims as amended, Applicant respectfully traverses the rejections for the reasons as follow.

Wong teaches an erasable and programmable read only memory (EEPROM) to store signals. In Wong, a floating gate 505 is formed on the gate dielectric layer with a uniform thickness. See cols. 6 and 7 and Fig. 5b of Wong. Furthermore, as shown in Fig. 6 of Wong, the floating gate can be further formed on a tunnel oxide layer, wherein the part of the floating formed above the tunnel oxide layer also has a uniform thickness.

MPEP 2131 prescribes that to anticipate a claim, a reference must teach every element of the claim. In this regard, the Federal Circuit has held:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).
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> "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Wong does not teach or suggest a stacked gate vertical flash memory comprising, *inter alia*, a conducting spacer formed on a dielectric layer as a floating gate, wherein the conducting spacer is tapered to a point at the gate dielectric layer, as recited in claim 1.

As amended, claim 1 recites a stacked gate vertical flash memory comprising a semiconductor substrate with a trench; a source conducting layer, formed on a bottom of the trench; an

insulating layer, formed on the source conducting layer a gate dielectric layer, formed on a sidewall of the trench; a conducting spacer, formed on the gate dielectric layer as a floating gate, wherein the conducting spacer is tapered to a point at the gate dielectric layer; an inter-gate dielectric layer, covered on the conducting spacer; and a conducting control gate filled in the trench.

Thus, in the invention recited in claim 1, the conducting spacer is tapered to a point at the gate dielectric layer to form a tip at the top of the conducting spacer. As noted in the specification, since the conducting spacer is tapered to a point, concentration of the electrical field easily occurs and the point discharge is increased, increasing the effects of erasure. Accordingly, the operation voltage may be decreased to 2/3 in programming or erasing of the stack gate with vertical tips in embodiments of the present invention. See page 8, line 25 to page 9, line 5 of the specification.

In the office action, the floating gates 505 and 605 are identified as the conducting spacer recited in claim 1. As noted previously, the thickness of floating gates 505 and 605 shown in Figs. 5b and 6 are uniform. Applicant therefore submits that Wong neither teaches nor suggests a stacked gate vertical flash memory comprising a conducting spacer formed on a dielectric layer as a floating gate, wherein the conducting spacer is tapered to a point at the gate dielectric layer. For at least this reason, claim 1 is believed to be allowable over Wong. Insofar as claims 2-13 depend from claim 1, it is Applicant's belief that these claims are also in condition for allowance.

Disqualification of Lin el al as Prior Art

Under 35 U.S.C. 103(c), subject matter developed by another person which is prior art under subsections 35 U.S.C. 102(e), (f) and (g) shall not preclude patentability under 35 U.S.C. 103 where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an assignment to the same person.

Statement Under 35 U.S.C 103(c)

Application No. 10/606,702 and U.S. Published Patent Application Serial No. 2004/0057328 were, at the time the invention of Application No. 10/606,702 was made, owned by Nanya Technology Corporation (Taoyuan, Taiwan).

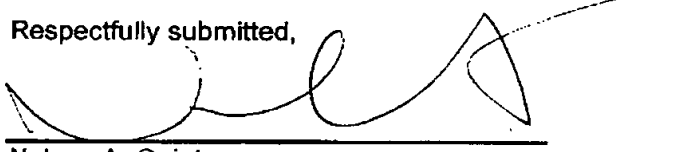
Rejections under 35 U.S.C. 103(a)

Claims 13-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Lin et al. Insofar as Lin et al is disqualified as prior art under 35 U.S.C. 103(a), it is Applicant's belief that these rejections are traversed and the claims 13-25 are in condition for allowance.

Conclusion

The Applicant believes that the application is now in condition for allowance and respectfully requests so. The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to Deposit Account No. **502447**. In particular, if this response is not timely filed, then the commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 C.F.R. § 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to Deposit Account No. **502447**.

Respectfully submitted,



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